Amendments to the Specification:

On page 1, at line 3, insert the following paragraph:

This application claims benefit of priority to French Patent Application No. FR 0216646 filed December 24, 2002, the disclosure of which is incorporated by reference herein.

On page 1, please insert the following heading at line 3:

TECHNICAL FIELD

On page 1, please insert the following heading at line 12:

BACKGROUND

On page 4, please insert the following heading at line 28:

SUMMARY

On page 13, please insert the following heading at line 31:

BRIEF DESCRIPTION OF THE DRAWING

On page 14, at line 1, please replace the paragraph with the following amended paragraph:

[[•]] ~~figures~~ FIGs. 1 to 4 are views in section of a wafer in the course of preparation with a view to fabrication of a mixed substrate,

On page 14, at line 4, please replace the paragraph with the following amended paragraph:

[[•]] ~~figures~~ FIGs. 5 to 7 are views in section of this mixed substrate during fabrication from the wafer of figures 1 to 4,

On page 14, at line 7, please replace the paragraph with the following amended paragraph:

[[•]] ~~figures~~ FIGs. 8 to 11 are views in section of another wafer in course of preparation with a view to fabrication of a second mixed substrate,

On page 14, at line 10, please replace the paragraph with the following amended paragraph:

[[•]] ~~figures~~ FIGs. 12 to 14 are views in section of this second mixed substrate during fabrication from the wafer of figures 8 to 11,

On page 14, at line 13, please replace the paragraph with the following amended paragraph:

[[•]] ~~figures~~ FIGs. 15 and 17 are views in section of the fabrication of two wafers intended for the fabrication of a mixed substrate of the type shown in figures 5 to 7,

On page 14, at line 16, please replace the paragraph with the following amended paragraph:

[[•]] ~~figures~~ FIGs. 18 to 24 are views in section analogous to figures 1 to 7 showing the preparation of the substrates from figure 17 and the fabrication of a mixed substrate therefrom,

On page 14, at line 20, please replace the paragraph with the following amended paragraph:

[[•]] ~~figures~~ FIGs. 25 to 27 are views in section of the fabrication of two wafers intended for the fabrication of a mixed substrate of the type shown in figures 12 to 14, and

On page 14, at line 23, please replace the paragraph with the following amended paragraph:

[[•]] ~~figures~~ FIGs. 28 to 34 are views in section analogous to figures 8 to 14 showing the preparation of the substrates from figure 27 and the fabrication of a mixed substrate therefrom.

On page 14, at line 27, please replace the paragraph with the following amended paragraph:

~~Figures~~ FIGs. 1 to 34 show several variants of the production of a mixed substrate in which impurity traps are distributed so as to have, in the bulk regions, an interface compatible with the production of bulk components.

On page 18, at line 2, please replace the paragraph with the following amended paragraph:

FIGs.~~Figures~~ 1 to 7 show a first embodiment of the invention.

On page 18, at line 12, please replace the paragraph with the following amended paragraph:

A 0.9 micron thick thermal oxide 11 is then generated over the whole of the surface (~~figure~~ FIG. 2). CMP (chemical mechanical polishing, see above) is used to polish this layer very flat to a thickness less than that of the layer 11, for example 0.7 micron (~~figure~~ FIG. 3). Accurate elimination is effected by monitoring the thickness to remove all (or practically all) of the thickness of oxide present over the regions Z2 (in fact there remains a thin layer of oxide that will be trapped at the time of the annealing); there remain oxide regions 11A (~~figure~~ FIG. 4). This elimination may be effected by wet treatment with HF, for example, or by further CMP treatment and/or hydrogen annealing and/or RIE treatment. The whole surface is then cleaned by heat treatment to render it hydrophobic.

On page 18, at line 27, please replace the paragraph with the following amended paragraph:

This wafer is then bonded by molecular adhesion to another silicon wafer 12 with no native oxide and whose surface is also hydrophobic (~~figure~~ FIG. 5).

On page 19, at line 1, please replace the paragraph with the following amended paragraph:

The second wafer is then thinned by mechanical and chemical abrasion, followed by polishing to obtain a mixed substrate including insulated - SOI - regions delimited by the regions Z1 and bulk regions of silicon-silicon contact delimited by the regions Z2 (~~figure~~ FIG. 6). These various regions may then be completely insulated from each other by trenches 14 (~~figure~~ FIG. 7).

On page 19, at line 23, please replace the paragraph with the following amended paragraph:

~~Figures~~ FIGs. 8 to 14 show a second embodiment of the invention.

On page 19, at line 25, please replace the paragraph with the following amended paragraph:

The starting wafer 20 is identical to that from ~~figures~~ FIGs. 1 to 7, except that its surface is coated with an oxide layer 1 micron thick. This wafer 20 is etched using a photolithographic mask with rectangular patterns until this oxide layer is completely removed in locations that are not masked. These etched regions are denoted Z1' and the non-etched regions are denoted Z2' (~~figure~~ FIG. 8); note that the thermal oxide forms in the silicon region Z'1 whereas it is impeded by the oxide in the region Z'2.

On page 19, at line 35, please replace the paragraph with the following amended paragraph:

A thermal oxide layer 21 0.8 micron thick is then formed over the whole of the surface (~~figure~~ FIG. 9) and the surface is then planarized by CMP, which entails removing a thickness of 1 micron (~~figure~~ FIG. 10).

On page 20, at line 4, please replace the paragraph with the following amended paragraph:

Precise elimination is effected by monitoring the thickness to remove all (or practically all) of the thickness of oxide on top of the regions Z'2 (~~figure~~ FIG. 11). This elimination may be effected by wet treatment with HF or by additional CMP treatment and/or hydrogen annealing and/or RIE. Localized layers 21A remain.

On page 20, at line 17, please replace the paragraph with the following amended paragraph:

Here, this second wafer 22 has been implanted with hydrogen ions with an energy of 76 keV and a dosage of 5×10^{16} at/cm^2 through an oxide layer 400 nm thick that is removed afterwards (~~figure~~ FIG.12), yielding a fragile layer 22A.

On page 20, at line 25, please replace the paragraph with the following amended paragraph:

This is followed by polishing to obtain a mixed substrate including SOI regions delimited by the regions Z1' and "bulk" silicon/silicon contact regions delimited by the regions Z2' (~~figure~~ FIG.13).

On page 20, at line 29, please replace the paragraph with the following amended paragraph:

These regions may then be insulated from each other by trenches 24 (~~figure~~ FIG. 14).

On page 20, at line 31, please replace the paragraph with the following amended paragraph:

~~Figures~~ FIGs.15 to 24 represent a third embodiment having analogies with the first embodiment.

On page 21, at line 4, please replace the paragraph with the following amended paragraph:

This wafer is then etched to produce graduated steps 32 consisting of rectangles 10 microns × 2 microns, repeated every 1/100° over two 20° circular arcs positioned on a circle of 90 mm diameter (~~figure~~ FIG.15).

On page 21, at line 8, please replace the paragraph with the following amended paragraph:

A second silicon wafer 33 with the same composition and the same dimensions as before is bonded by hydrophilic molecular adhesion to the first wafer (~~figure~~ FIG. 16).

On page 21, at line 11, please replace the paragraph with the following amended paragraph:

Fracture in the implanted region is caused by mechanical and/or heat treatment of any appropriate type known in the art; two wafers 40 and 42 are obtained of which one, of SOI type, is referred to hereinafter as the "positive" wafer while the other is referred to as the "negative" wafer (~~figure~~ FIG. 17).

On page 21, at line 17, please replace the paragraph with the following amended paragraph:

The wafer 40 is subjected to the same processing steps as the wafer 10 (figures 18 to 21 correspond to ~~figures~~ FIGs. 1 to 4) with generation of an oxide layer 41 by deposition or by thermal oxidation, until a hydrophobic surface is obtained including localized oxide regions 41A (~~figure~~ FIG.21).

On page 21, at line 23, please replace the paragraph with the following amended paragraph:

This wafer is then bonded by molecular adhesion to the positive wafer 42 which has no native oxide and whose surface is also hydrophobic (~~figure~~ FIG. 22).

On page 22, at line 3, please replace the paragraph with the following amended paragraph:

After stabilization annealing (at 1300°C for 3 hours), the "positive" wafer is thinned by mechanical and chemical abrasion using the buried oxide layer of the "positive" wafer as the stop layer. This stop layer is then removed to obtain a mixed substrate including SOI regions delimited by the regions Z1" and silicon/silicon contact regions delimited by the regions Z2" (~~figure~~ FIG.23). These various regions may be insulated from each other by trenches 44 (~~figure~~ FIG.24).

On page 22, at line 19, please replace the paragraph with the following amended paragraph:

F~~igures~~ FIGs.25 to 34 show a fourth embodiment having analogies with the second embodiment.

On page 22, at line 26, please replace the paragraph with the following amended paragraph:

The same type of etching is then carried out as in this third embodiment to form steps 52 (~~figure~~ FIG.25).

On page 22, at line 28, please replace the paragraph with the following amended paragraph:

A second wafer 53 of the same kind and with the same dimensions as the preceding wafers is bonded by hydrophilic molecular adhesion to the first wafer (~~figure~~ FIG.26) and fracture is caused in the implanted region, as in this third embodiment, to obtain a so-called "negative" wafer 60 and a so-called "positive" wafer 62 (~~figure~~ FIG. 27).

On page 22, at line 34, please replace the paragraph with the following amended paragraph:

The "negative" wafer is then oxidized over the whole of its surface, like the wafer 20 of the second embodiment, to form an oxide layer 1 micron thick. This last wafer is then etched like the wafer 20 (~~figure~~ FIG. 28) and a thermal oxide layer 61 that is 0.8 micron thick is deposited (~~figure~~ FIG. 29). The same treatments are applied as are applied to the wafer 20 (~~figures~~ FIGs. 28 to 34 are analogous to ~~figures~~ FIGs. 8 to 14), to render the surface hydrophilic, with localized oxide regions 61A.

On page 23, at line 1, please replace the paragraph with the following amended paragraph:

The second bonding is effected with the minimum misalignment between the two crystals by aligning the graduated steps, as in the third embodiment (~~figure~~ FIG. 32).